

DERWENT-ACC-NO: 2001-352889
DERWENT-WEEK: 200137
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TITLE: Method of wafer level package and structure thereof
- utilize two
elastic layers for buffering thereby producing a package
structure with a low
cost and a high reliability

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PATENT-ASSIGNEE: IND TECHNOLOGY RES INST[INTEN]

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PATENT-FAMILY:

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INT-CL_(IPC): H01L021/00

ABSTRACTED-PUB-NO: TW 419712A

BASIC-ABSTRACT: NOVELTY - The present invention discloses a method for a wafer level package and a structure thereof. The method comprises: directly packaging the whole wafer; cutting the package to form a single chip package; providing a silicon wafer with a plurality of IC chips in which the I/O pad of each chip is formed with a conductive metal pillar; separately using two elastic layers, in which one layer is coated on the whole wafer to expose the surface of the metal pillar, and the other layer is printed on a portion of the

first elastic layer; forming metal lines to realize the redistribution of the port ends so that one end extends onto the second elastic layer to form an I/O pad with a periphery arrangement or a face matrix arrangement; and implanting a solder ball on the I/O pad of the second elastic layer. The present invention utilizes two elastic layers for buffering thereby producing a package structure with a low cost and a high reliability.

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS:

METHOD WAFER LEVEL PACKAGE STRUCTURE TWO ELASTIC LAYER
BUFFER PRODUCE PACKAGE
STRUCTURE LOW COST HIGH RELIABILITY

DERWENT-CLASS: U11

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